

REVIEW OF FULL ADDER USING REVERSIBLE LOGIC

SEEMA RAJPUT¹, RITA JAIN² & AWADHESH K. G. KANDU³

¹Research Scholar, Department of Electronics & Communication LNCT, Bhopal, Madhya Pradesh, India

²HOD EC, Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, India

³Assistance Professor, Lakshmi Narain College of Technology, Bhopal, Madhya Pradesh, India

ABSTRACT

In the field of cryptography, optical information processing low power CMOS design and nanotechnology Reversible logic has found its applications and has become one of the promising research directions This paper presents a novel and quantum cost efficient reversible full adder gate in nanotechnology. This gate can work singly as a reversible full adder unit and requires only one clock cycle. The proposed gate is a universal gate in the sense that it can be used to synthesize any arbitrary Boolean functions. It has been demonstrated that the hardware complexity offered by the proposed gate is less than the existing counterparts. The proposed reversible full adder is then compared with the adder and the floating point adder.

KEYWORDS: Component, Floating Point Adder, Reversible Logic